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10EC45

Fourth Semester B.E. Degree Examination, June/July 2018
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions, selecting at least TWO full questions from each part.***

PART – A

1 a. Explain VHDL and verilog ports. **(07 Marks)**

b. Discuss scalar data types in aVHDL. **(08 Marks)**

c. Compare VHDL and verilog. **(05 Marks)**

2 a. List five major differences between signal assignment and variable assignment statements. **(05 Marks)**

b. Draw the logic symbol and excitation table of a D-latch. Derive the next state equation and draw the logic diagram. Write verilog code in dataflow description. **(10 Marks)**

c. Explain, with example, how to assign delay time to signal assignment statements in VHDL and verilog. **(05 Marks)**

3 a. Explain process statement in VHDL and always statement in verilog. **(08 Marks)**

b. Write behavioral verilog code for a 8:3 priority encoder. **(06 Marks)**

c. Multiply +7 and -5 using Booth's algorithm. **(06 Marks)**

4 a. Explain with example, i) Binding between library and component in VHDL and ii) Binding between two modules in verilog. **(10 Marks)**

b. Write VHDL structural description of a N-bit magnitude comparator using generate statement (Assume all component descriptions available in work library). **(10 Marks)**

PART – B

5 a. Explain procedures in VHDL and tasks in verilog. **(06 Marks)**

b. Write verilog code to convert an unsigned integer to binary using task. **(06 Marks)**

c. Write VHDL description using function to compute the factorial of a positive integer. **(08 Marks)**

6 a. Describe packages in VHDL with example. **(06 Marks)**

b. Draw the block diagram and write verilog description for a 16 × 8 SRAM. **(10 Marks)**

c. List various built-in procedures and built-in tasks for file-handling. **(04 Marks)**

7 a. Develop a block diagram of a 9-bit adder using three 3-bit carry look-ahead adder slices. Describe 3-bit look-ahead adder slice using VHDL and invoke this in verilog module. **(10 Marks)**

b. Show through an example of 8:3 priority encoder how to instantiate CASEX in VHDL. **(10 Marks)**

8 a. What is synthesis? Discuss important facts associated with synthesis. **(08 Marks)**

b. Generate the gate-level synthesis for a signal assignment statement y = 2 * x + 3 and write its structural code in verilog. **(12 Marks)**

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Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.